IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Eitan Rosen	Art Unit	: 2116
Serial No.	: 10/631,327	Examiner	: Tse W. Chen
Filed	: July 30, 2003	Conf. No.	: 1395
Title	: DDR INTERFACE BUS CONTROL		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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BRIEF ON APPEAL

Applicant files this brief on appeal under 37 C.F.R. § 41.37, in response to the Final Office Action mailed on October 10, 2008.

The section required by 37 C.F.R. § 41.37 follows.

(1) Real Party in Interest

Marvell Semiconductor, Inc., the assignee of this patent application, is the real party in interest.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

Claims 1-15 and 23-37 are pending in the action, with claims 1 and 23 being independent. Claims 16-22 were canceled during prosecution.

Applicant appeals the rejection of claims 1-15 and 23-37.

(4) Status of Amendments

The claims have not been amended subsequent to the Final Office Action mailed October 10, 2008, and there are no unentered amendments.

(5) Summary of Claimed Subject Matter

Claim 1

Claim Language	Support in Specification and/or FIGS.
A circuit, comprising:	*See e.g.*, FIG. 3.
a clock transmitter in communication with a clock bus, the clock transmitter to transmit a clock signal on the clock bus;	*See e.g.*, first device 310 and DQS bus 330 shown in FIG. 3.
a clock receiver in communication with the clock bus, the clock receiver to receive a clock signal on the clock bus; and	*See e.g.*, second device 320 shown in FIG. 3.
a driver in communication with the clock bus, the driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.	*See e.g.*, driver 350 shown in FIG. 3; *see also* [0026] and [0027].

Claim 23

Claim Language	Support in Specification and/or FIGS.
A circuit, comprising:	*See e.g.*, FIG. 3.
a clock signal transmission means in communication with a clock bus, the clock signal transmission means for transmitting a clock signal on the clock bus;	*See e.g.*, first device 310 and DQS bus 330 shown in FIG. 3.
a clock signal receiving means in communication with the clock bus, the clock signal receiving means for receiving a clock signal on the clock bus; and	*See e.g.*, second device 320 shown in FIG. 3.
a voltage driving means in communication with the clock bus, the voltage driving means for driving and maintaining a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.	*See e.g.*, driver 350 shown in FIG. 3; *see also* [0026] and [0027].

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-3, 5-6, 23-25 and 27-28 are rejected under 35 U.S.C. §102(b) as being

anticipated by US Pub. No. 2004/0019816 to **Smith**.

Claims 4 and 26 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of USP No. 5,732,249 to **Masuda**.

Claims 7 and 29 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of USP No. 5,355,468 to **McDaniel**.

Claims 8-10 and 30-32 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of USP No. 5,355,468 to **Jeppesen**.

Claims 11-15 and 33-37 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of USP No. 5,964,856 to **Wu**.

Applicant respectfully requests that these rejected claims be reviewed on appeal.

(7) Argument

Section 102(e) Rejections

Claims 1-3, 5-6, 23-25 and 27-28 are rejected under 35 U.S.C. §102(e) as being anticipated by US Pub. No. 2004/0019816 to **Smith**. Applicant respectfully traverses these rejections.

Claim 1 recites in part a driver to **drive and maintain** a voltage of the clock bus while a clock transmitter is not transmitting a clock signal on the clock bus and a clock receiver is not receiving a clock signal on the clock bus.

In the Office Action mailed June 4, 2008 ("Office Action"), the Examiner asserted that Smith provides a driver that drives and maintains a voltage of a clock bus at paragraph [0021]. *See* page 2, item 3, lines 6-9 of the Office Action. This paragraph reads

> **[0021]** The RCLK line **208** of circuit **202** is connected to a voltage source **210** through a current limiting resistor **212**. The master **214** is connected to the RCLK line **208** through an amplifier **216** and a pull down transistor **218**. The slave **220** is connected to the RCLK line **208** through an amplifier **222** only. In the normal idle state, RCLK **208** is high and can be pulled low only by the master **214**. The slave **220** may only monitor RCLK **208** through the amplifier **222**.

In the "Response to Argument" section of the Final Office Action dated October 10, 2008 ("Final Office Action"), the Examiner supplemented his previous position and asserted that the claimed features are "already disclosed in prior art in figure 2 of Applicant's own application".

See page 8, lines 1-2 of the Final Office Action.

I. The Examiner's reliance on the AAPA is not proper

a. The AAPA has not been officially cited

As a preliminary matter, the Examiner has not officially cited Applicant's admitted prior art ("AAPA") in rejecting the pending claims. As such, Applicant respectfully submits that the Examiner's reliance on the AAPA is improper, and that the AAPA cannot be used as an evidentiary showing to support the current ground of rejection—a plain legal error.

b. The AAPA fails to teach or suggest a driver

Even assuming *arguendo* that the Examiner's unofficial reliance on the AAPA is proper, as discussed in the Background, after data transmission by a transmitting device 110 to a receiving device 120, the voltage of the clock bus 130 drifts to a voltage that "corresponds to neither a logical one nor a logical zero." *See* [0007]. Applicant respectfully submits that this unknown state, as shown in FIG. 2, causes confusion (e.g., with respect to the receiving device 120) as to the availability of the clock bus 130 because the voltage of the clock bus 130 is not, for example, driven to or maintained at a particular voltage to prevent voltage drifting. *Id.*

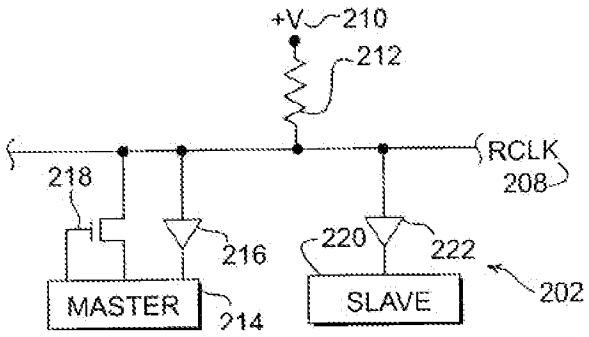
Further, the fact that the AAPA does not utilize any driver (*see e.g.*, the first device 110 shown in FIG. 1) also supports that the clock bus 130 is neither driven nor maintained at a particular voltage. Rather, the voltage of the AAPA's clock bus 130 fluctuates and drifts to a state unknown to the transmitting device 110 and the receiving device 120. *See* [0007].

II. Smith also fails to teach or suggest Applicant's claimed driver

In order to address paragraph [0021] of Smith relied upon by the Examiner as allegedly disclosing the claimed features, Applicant first provides an overview of Smith.

Smith provides a three-wire-serial bus that connects between a master 214 and one or more slaves 220. *See* [0020]. The three-wire-serial bus includes an acknowledgement line RACK, a data line RDAT and a clock line RCLK 208. *Id.*

FIGURE 2A

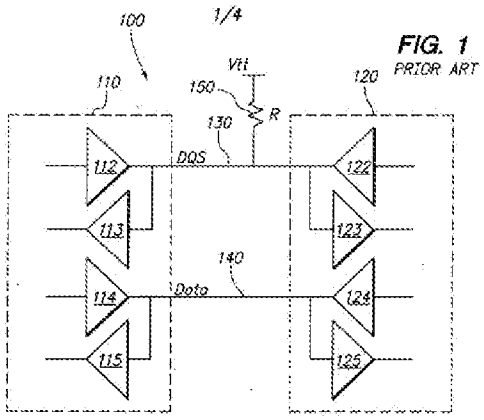


Referring to FIG. 2A above, in a normal idle state (a state where no communication occurs; *see* [0046]), Smith's clock line RCLK 208 floats HIGH. *See* [0021]. To commence an exchange of data between the master 214 and the slave(s) 220, the master 214 first receives an acknowledgement (e.g., via the RACK line) from each slave that data transmission can commence. *See* [0036]. For example, the last slave to release the RACK line indicates that every slave has acknowledged the data request. *See* [0034]. Then, the master 214 releases, *inter alia*, the clock line RCLK 208 by pulling the clock line RCLK 208 LOW to allow data to be exchanged between the master 214 and the slaves 220. *See* [0021].

a. Smith does not drive the voltage of the clock line RCLK to a particular voltage level or maintain the voltage of the clock line RCLK at that voltage level

Applicant respectfully submits that Smith does not drive and maintain the voltage of the clock line RCLK 208 to a particular voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus. Smith's clock line RCLK 208 normally floats HIGH when not in use due to the pull up. *See* [0008]. The clock line RCLK 402 then floats back to HIGH when data transmission is complete (*see* periods 436-442). *See* [0030]. Applicant respectfully asserts, the Smith structure is similar to the AAPA's structure and accordingly Smith does not drive the clock line RCLK 208 **to** a voltage level. *Id.*

b. Smith is cumulative to the AAPA



In the AAPA, a terminating voltage source V_{tt} is used that connects to the clock bus 130 as shown in FIG. 1 above. However, as discussed in the AAPA, the clock bus 130 still drifts away from a known state, causing instability to the clock bus 130 and uncertainty as to whether the clock bus 130 is available, particularly when no data is being exchanged between the transmitting device 110 and the receiving device 120. *See* [0007].

Similarly, Smith provides a voltage source 210 connected to a current limiting resistor 212. *See* [0021]. Smith, however, does not express any particular function of the voltage source 210. All we know is that Smith's voltage source 210 is connected to the clock line RCLK 208. In this regard, Smith, at best, is merely cumulative to the AAPA described on pages 1-3 of Applicant's specification in that Smith's voltage on the clock line RCLK 208 is also subject to drifting to an unknown state even if Smith employs a voltage source 210. Smith's voltage source 210 is not Applicant's claimed driver, as Smith's voltage source 210 does not, for example, drive the clock line RCLK 208 to a voltage level or maintain the clock line RCLK 208 at the voltage level thereafter. *See* [0037]. By contrast, Applicant's claimed driver drives and maintains the voltage of a clock bus to a first voltage level so that a device can determine the availability of the clock bus, for example, by recognizing a change in voltage of the clock bus (e.g., from a voltage value corresponding to a logical "1" to a voltage value corresponding to a logical "0"). Smith recognizes a start of a data transmission only after handshaking has been performed through locking and releasing the clock line RCLK 208, whereas Applicant's claimed driver recognizes the availability of a clock bus based on the voltage level of the clock bus.

It is plain legal error to read a feature entirely out of a claim, or to ignore a feature positively recited in a claim. *Maxwell v. J. Baker, Inc.*, 86 F.3d 1098, 1105 (Fed. Cir. 1996) (refusing to adopt a claim construction that would ignore a claim limitation); *see also Texas*

Instruments Inc. v. U.S. Int'l Trade Comm'n, 988 F.2d 1165, 1171 (Fed.Cir.1993) ("construing the claims in the manner suggested by TI would read an express limitation out of the claims. This we will not do...."). As the Examiner has not provided any consideration to Applicant's claimed "driving and maintaining a voltage of a clock bus to a first voltage level", Applicant respectfully submits that Smith does not anticipate claim 1.

Claims 2-3 and 5-6 depend from claim 1, and also are submitted to be allowable for at least the reasons discussed with respect to claim 1.

Claim 23

Claim 23 recites in part a voltage driving means for driving and maintaining a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

As discussed above, Smith does not teach or suggest at least these features. For at least these reasons, Applicant respectfully submits that Smith also does not anticipate claim 23.

Claims 24-25 and 27-28 depend from claim 23, and also are submitted to be allowable for at least the reasons discussed above with respect to claim 23.

Section 103(a) Rejections

Claims 4 and 26 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of **Masuda**. Claim 4 depends from claim 1 and claim 26 depends from claim 23. Claims 4 and 26 are submitted to be allowable for at least the reasons discussed above with respect to claims 1 and 23, respectively.

Claims 7 and 29 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of **McDaniel**. Claim 7 depends from claim 1 and claim 29 depends from claim 23. Claims 7 and 29 are submitted to be allowable for at least the reasons discussed above with respect to claims 1 and 23, respectively.

Claims 8-10 and 30-32 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of **Jeppesen**. Claims 8-10 depend from claim 1 and claims 30-32 depends from claim 23. Claims 8-10 and claims 30-32 are submitted to be allowable for at

least the reasons discussed above with respect to claims 1 and 23, respectively.

Claims 11-15 and 33-37 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Smith** in view of **Wu**. Claims 11-15 and claims 33-37 are submitted to be allowable for at least the reasons discussed above with respect to claims 1 and 23, respectively.

Finality of the Office Action is Precluded

Applicant notes the Examiner has rendered the Office Action mailed October 10, 2008 "Final". Applicant respectfully submits that it is plain legal error to render a finality to this Office Action because the Office Action contains new objections (e.g., objections to the drawings) that were neither "necessitated by a claim amendment or based on information from an information disclosure statement." *See* M.P.E.P. §706.07(a). By issuing a finality, prosecution on the merits is closed, and Applicant is precluded from, for example, presenting evidence to demonstrate that the new objections are improper, or alternatively, submitting new changes to address the new objections. Applicant submits that the new objections effectively shift the burden to the Applicant; however, the preclusion takes away, from the Applicant, an opportunity to address the objection or provide remedy thereto. For at least these reasons, Applicant respectfully submits that the finality of the Office Action is improper.

Objections to the Drawings

The drawings are objected to under 37 C.F.R. §1.83(a). Specifically, the Examiner asserts that the limitation "driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus" is not shown in the drawings. *See* page 2, item 1, lines 1-6 of the Final Office Action.

Applicant respectfully submits that the claimed features are shown in FIG. 4. For example, referring to FIG. 4 and as discussed in paragraphs [0025]-[0027] and [0030]-[0031] of the specification, data may be transmitted between a first device 310 (e.g., a packet device) and a second device 320 (e.g., memory) (see FIG. 3). A data strobe (DQS) driver 350 may be used to drive a clock signal on a DQS bus 330. As shown in FIG. 4, at time t_0, the first device 310 may transmit data to the second device 320 and relinquish control of the DQS bus 330 at time t_1. The

driver 350 then pulls the voltage on the DQS bus 330 to a logical one. Until time t_2 has been reached, the voltage of the DQS bus 330 is driven and maintained at logical one. (e.g., driving and maintaining the DQS bus 330 at logical one when the first device 310 is not transmitting). At time t_2, the second device 320 then takes control of the DQS bus 330, as shown in FIG. 4 by the change of logical one to logical zero.

For at least these reasons, Applicant respectfully requests that the objection to the drawings be withdrawn on appeal.

The brief fee of $540 is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: January 30, 2009

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Appendix of Claims

1. A circuit, comprising:

a clock transmitter in communication with a clock bus, the clock transmitter to transmit a clock signal on the clock bus;

a clock receiver in communication with the clock bus, the clock receiver to receive a clock signal on the clock bus; and

a driver in communication with the clock bus, the driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

2. The circuit of claim 1, wherein the first voltage level is a voltage level corresponding to a logical one.

3. The circuit of claim 1, wherein the driver includes a resistance.

4. The circuit of claim 3, wherein the driver includes a first resistance between the clock bus and a voltage VDD, and wherein the driver further includes a second resistance between the clock bus and ground.

5. The circuit of claim 1, wherein the driver includes a transistor.

6. The circuit of claim 1, further including enabling circuitry in communication with the driver, the enabling circuitry to enable the driver when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

7. The circuit of claim 6, the enabling circuitry further to disable the driver when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

8. The circuit of claim 6, further including receive processing circuitry in communication with the enabling circuitry, the receive processing circuitry including a receive processing clock, the receive processing clock to turn off in response to a signal from the enabling circuitry.

9. The circuit of claim 6, wherein the enabling circuitry includes a flip flop.

10. The circuit of claim 9, wherein the enabling circuitry enables the driver when the flip flop is in a first state, and wherein the enabling circuitry disables the driver when the flip flop is in a second state.

11. The circuit of claim 1, wherein the driver is included in a packet processor.

12. The circuit of claim 1, wherein the driver is included in a packet processor configured to transmit data and to receive data according to a double data rate protocol.

13. The circuit of claim 12, further including a memory.

14. The circuit of claim 13, wherein the memory is configured to transmit data and to receive data according to the double data rate protocol.

15. The circuit of claim 13, wherein the memory includes:

another clock transmitter in communication with the clock bus, the another clock transmitter to transmit a clock signal on the clock bus;

another clock receiver in communication with the clock bus, the another clock receiver to receive a clock signal on the clock bus; and

another driver in communication with the clock bus, the another driver to drive the voltage of the clock bus to the first voltage level when the another clock transmitter is not transmitting a clock signal on the clock bus and the another clock receiver is not receiving a clock signal on the clock bus.

16-22. (Canceled)

23. A circuit, comprising:

a clock signal transmission means in communication with a clock bus, the clock signal transmission means for transmitting a clock signal on the clock bus;

a clock signal receiving means in communication with the clock bus, the clock signal receiving means for receiving a clock signal on the clock bus; and

a voltage driving means in communication with the clock bus, the voltage driving means for driving and maintaining a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

24. The circuit of claim 23, wherein the first voltage level is a voltage level corresponding to a logical one.

25. The circuit of claim 23, wherein the voltage driving means includes a resistance means.

26. The circuit of claim 25, wherein the voltage driving means includes a first resistance means between the clock bus and a voltage VDD, and wherein the voltage driving means further includes a second resistance means between the clock bus and ground.

27. The circuit of claim 23, wherein the voltage driving means includes a transistor.

28. The circuit of claim 23, further including enabling means in communication with the voltage driving means, the enabling means for enabling the voltage driving means when the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

29. The circuit of claim 28, the enabling means further for disabling the voltage driving means when the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

30. The circuit of claim 28, further including receive processing means in communication with the enabling means, the receive processing means including a receive processing clock means, the receive processing clock means to turn off in response to a signal from the enabling means.

31. The circuit of claim 28, wherein the enabling means includes a flip flop.

32. The circuit of claim 31, wherein the enabling means enables the driving means when the flip flop is in a first state, and wherein the enabling means disables the driver when the flip flop is in a second state.

33. The circuit of claim 23, wherein the voltage driving means is included in a packet processing means.

34. The circuit of claim 33, wherein the packet processing means is for transmitting data and for receiving data according to a double data rate protocol.

35. The circuit of claim 34, further including a memory means.

36. The circuit of claim 35, wherein the memory means is for transmitting data and for receiving data according to the double data rate protocol.

37. The circuit of claim 35, wherein the memory means includes:

another clock signal transmission means in communication with a clock bus, the another clock signal transmission means for transmitting a clock signal on the clock bus;

another clock signal receiving means in communication with the clock bus, the another clock signal receiving means for receiving a clock signal on the clock bus; and

another voltage driving means in communication with the clock bus, the another voltage driving means for driving a voltage of the clock bus to a first voltage level when the another clock signal transmission means is not transmitting a clock signal on the clock bus and the another clock signal receiving means is not receiving a clock signal on the clock bus.

Evidence Appendix

None.

Related Proceedings Appendix

None.